Modeling of Planar Varactor Frequency Multiplier Devices with Blocking Barriers

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***Abstract*—Models for optimization of planar frequency triplers with symmetrical $C - V$ curves are presented. Role and limitation of various blocking barriers (oxide, Mott, heterojunction) are discussed. Devices with undoped drift regions (BIN) have moderate efficiency but a broad range of power operation, whereas devices with doped drift regions (BNN) have high efficiency in a narrow power window. In particular, an upper power limit of the BNN is caused by electron velocity saturation. Implementations in SiO_2/Si and AlAs/GaAs and means for increasing the power of BNN structures are considered.**

I. Introduction

WHISKER-contacted gallium arsenide Schottky barrier varactor diodes are the classical devices for frequency multiplication in the microwave region. During the last two decades efforts have been made to adapt this device for operation in the near-millimeter wave region. The most important improvement was the introduction of a moderately doped epitaxial layer on a heavily doped substrate for reduction of series resistance without loss of capacitance swing. Recently [17] an output power of 0.7 mW at 500 GHz has been achieved with such a diode in a frequency tripler with an efficiency of 2%. However, the device is still hampered by the following disadvantages:

1) There is still a substantial parasitic series resistance due to the ohmic back contact and the relatively long path from that contact to the active layer, especially when the skin effect becomes important.

2) Mainly the second harmonic is generated so that for higher order multiplication expensive idler circuits must be provided.

3) The whisker contact poses a reliability problem and is not suitable for quasi-optically coupled diode arrays.

4) The multiplication efficiency degrades seriously with increasing power when the electrons approach their saturation velocity.

In the following we will explore concepts of varactors with electron blocking barriers which promise to overcome or improve on those shortcomings. The Schottky barrier is replaced by a modified barrier involving a positive charge sheet that enables the device to reach a maximum capacitance at an arbitrary reverse bias. If two such diodes are connected in antiseries, a symmetrical pulse-like capacitance-voltage, $C - V$, curve with a large capacitance swing is obtained, which generates only odd harmonics without idlers.[1] By integrating two diodes back-to-back on one chip, the ohmic contacts are eliminated.

Fig. 1 shows the device structure and its equivalent circuit. Each diode is constructed, top to bottom, of a Schottky metal contact, the barrier with a thickness $d_{bar} \approx 10 \cdots 30$ nm, an N-type doping sheet, a drift region $d_{drift} \approx 50 \cdots 150$ nm, and an N^+ back contact connecting the two diodes. No bias is required as the sheet doping controls the operating point of the diodes. Thanks to the favorable geometry the parasitic series resistance is minimal and does not degrade due to skin effect. Lateral isolation can be achieved by mesa etching and deposition of SiO_2. An additional light etch after metal deposition is recommended in order to reduce near-surface leakage between the metal contacts. An optional etch stop layer [18] allows the removal of the substrate for minimizing the parasitic capacitance and transmission line losses of the leads. The simple, high-yield planar process is appropriate for high-reliability hybrid integration of single devices with planar waveguide coupling and filter structures as well as for on-chip integration with planar antennas in quasi-optically coupled multidiode arrays [14].

Following the historical development, we will analyze diodes with different types of active regions. The first arrangement is the Barrier-Intrinsic-N^+ (BIN) and the second the Barrier-N-N^+ (BNN) diode. Based on these analyses we will propose a third arrangement, the Multiple Barrier-N-Barrier (BNB) diode. The theoretical models presented here are not intended to be rigorous but rather to serve as guides to the prototype design of such structures. In this spirit, an intrinsic cut-off frequency is estimated for each type of diode from the minimum series

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[1]No useful capacitance swing would be obtained from Schottky varactor diodes in antiseries as such diodes are already largely depleted at zero bias.

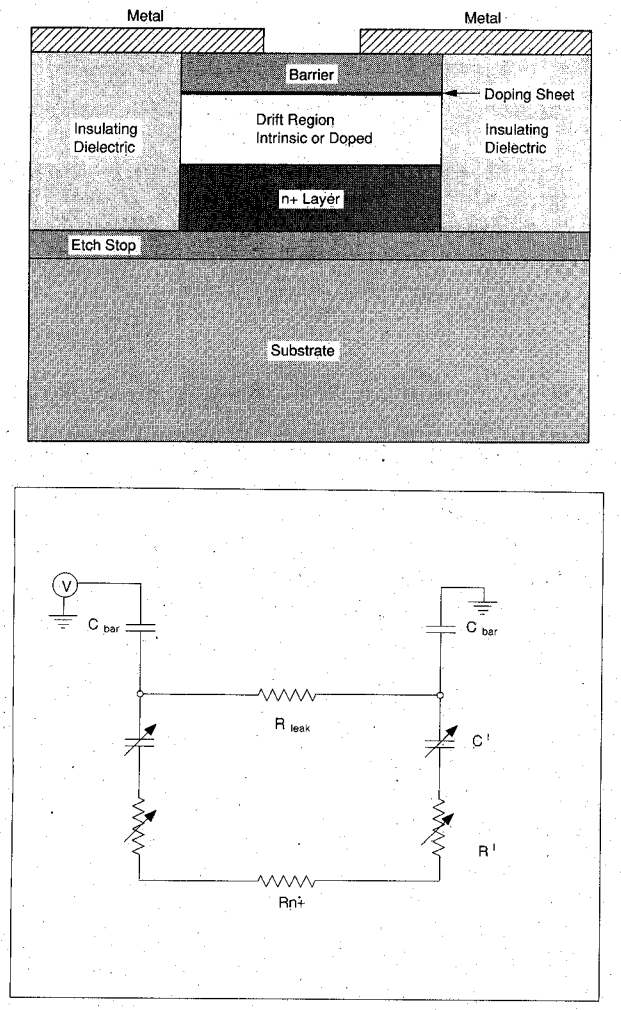

Fig. 1. Planar blocking barrier varactor: cross section (top) and equivalent circuit (bottom).

capacitance of the drift layer, $C'_{\min}$, occurring in depletion, and its maximum series resistance, $R'_{\max}$, occurring in accumulation, as

$$\omega_{ci} = 1/R'_{\max} C'_{\min}. \tag{1}$$

Parasitic series resistance must be added to $R'_{\max}$ for calculation of the extrinsic cut-off frequency. In reality, time averages of series capacitance and resistance affect the harmonic generation of the diodes making it dependent on the signal waveforms and thus on the embedding and driving conditions.

II. Barrier-Intrinsic-N$^+$ (BIN) Multipliers

If the drift region is intrinsic (I), electrons injected from the N^+ back contact carry a space charge limited current and accumulate at the blocking barrier. The $C - V$ characteristic in this case has a steep transition, $dC/C\,dV = q/kT$, between minimum and maximum capacitance enabling this "space charge varactor" [1], [6], [9] to generate a frequency spectrum of high harmonic content suitable for triplers and higher order multipliers even at low power levels. With

TABLE I
Calculated Intrinsic Cut-Off Frequency for $d_{\text{drift}} = 100$ nm and $N = 10^{17}/\text{cm}^3$

	ϵ/ϵ_0	$\mu(N)$ [cm^2/Vs]	v_s [cm/s]	$E_{\text{crit}}(N)$ [kV/cm]	f_{ci}(BIN) [GHz]	f_{ci}(BNN) [THz]
Si	12	700	1×10^7	15	300	1.5
GaAs	13	4500	$1 \cdots 2 \times 10^7$	$2 \cdots 4$	$300 \cdots 600$	8.6

$$C'_{\min} = \epsilon_{\text{drift}} A/d_{\text{drift}} \tag{2}$$

and the high-field approximation [6]

$$R'_{\max} = d^2_{\text{drift}}/2\epsilon_{\text{drift}} v_s A, \tag{3}$$

one obtains

$$\omega_{ci} = 2v_s/d_{\text{drift}}, \tag{4}$$

where A is the area of a single diode and v_s is the effective electron saturation velocity, which may depend on d_{drift} and the field distribution. As d_{drift}/v_s represents the average time needed by an electron to cross the drift region, the response of the BIN diode is transit-time limited and does not depend on the electron concentration. Estimates of the value of the average electron velocity in 100 nm GaAs layers range from 0.6×10^7 cm/s for space averaging [10] to 3×10^7 cm/s for time averaging [11]. A simulation for transit time devices [12] gave values $1 \cdots 2 \times 10^7$ cm/s. Similar values have been calculated for Si [15] so that the advantage of GaAs in the BIN application seems to be questionable. Table I lists the calculated intrinsic cut-off frequencies.

The validity of the BIN concept was proven with a single, whisker-coupled SiO_2/Si diode operating as a frequency doubler in a crossed waveguide [2] and performing closely to the predictions of a large signal analysis for a stepfunction $C - V$ [3], as shown in Fig. 2. The area dependence of the efficiency originates from the area dependence of the cut-off frequency through the parasitic spreading and back contact resistances. The figure shows also the performance of a (not optimal) epitaxial GaAs Schottky barrier mixer diode tested in the same waveguide mount.

Unfortunately, an extension of that theory [3] to pulse-like $C - V$ characteristics [4], as exhibited by back-to-back BIN diodes, proved to be unrealistic. Therefore we resorted to a simulator [5], shown in Fig. 3, which allows the device to be described by an arbitrary $C(V_C)$ curve, where V_C denotes the voltage drop over the capacitance only, and a fixed series resistance R. The program optimizes the embedding impedances at input and output frequencies for a given input power P_{in} in order to find the maximum output power P_{out}.

Fig. 4 shows a schematic $C - V$ curve from a back-to-back BIN with its characteristic values related to physical diode properties as follows. The maximum capacitance is reached when both diodes are in accumulation, whereas the minimum capacitance occurs when one diode is in accumulation and the other fully depleted, leading to

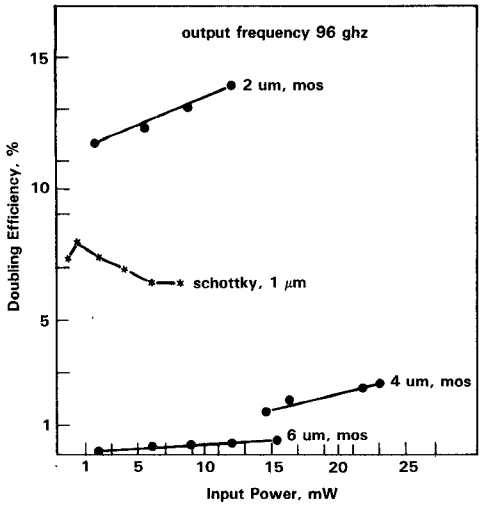

Fig. 2. Measured [2] efficiencies for frequency doubling in crossed waveguides of single, whisker-coupled MOS BIN diodes with d_{bar} = 10 nm, d_{drift} = 100 nm, and different front metal contact radii. Theory [3] predicts a maximum efficiency of 17% for the smallest diode. Non-optimal Schottky barrier mixer diode tested in same mount.

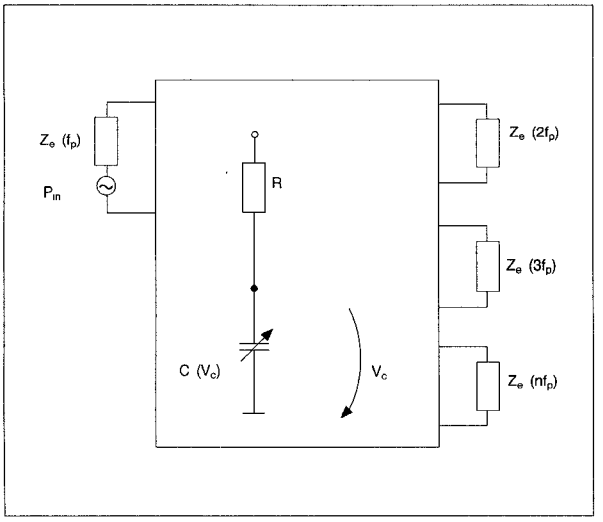

Fig. 3. Varactor multiplier signal simulator with embedding impedances Z_e at fundamental f_p and harmonics. For tripler $\Re\{Z_e(nf_p)\} \gg R$ for n = 2, 4, 5, 6, 7 was chosen. Simulator maximizes output power by optimizing $Z_e(f_p) = R_1 + jX_1$ and $Z_e(3f_p) = R_3 + jX_3$.

$$C_{max} = C_{bar}/2 \tag{5}$$

and

$$C_{min} = \frac{C'_{min} C_{bar}/2}{C'_{min} + C_{bar}/2} \tag{6}$$

with $C_{bar} = \epsilon_{bar} A/d_{bar}$. The halfwidth of the $C - V$ curve is close to $2V_f$, where V_f is called flatband voltage because at that voltage the field at the barrier is zero, marking the transition between accumulation and depletion of the drift region. For the most general case of a trapezoidal barrier, see Fig. 5, the flatband voltage is determined from the sheet doping, N_{sheet}, together with the barrier height at the metal interface, Φ_M, the barrier height at the interface with the drift material, Φ_D, and a small potential step at the

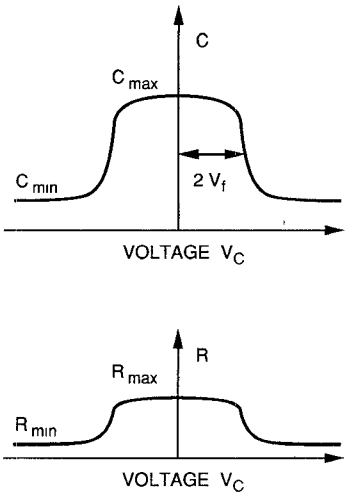

Fig. 4. Capacitance and series resistance of back-to-back BIN diodes as function of voltage drop over capacitance. Halfwidth equals twice the flatband voltage of single diode.

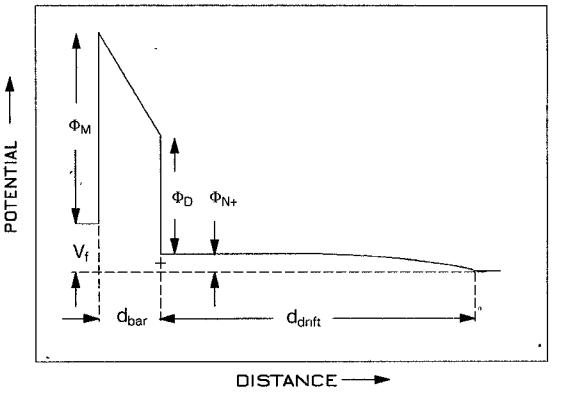

Fig. 5. Electron potential of single BIN diode with a trapezoidal barrier, biased at flatband voltage, V_f. The field discontinuity between barrier and drift region is controlled by a doping sheet (+) close to that interface.

border between drift and N^+ region Φ_{N+} as

$$V_f = qN_{sheet} d_{bar}/\epsilon_{bar} + \Phi_D - \Phi_M + \Phi_{N+}, \tag{7}$$

where [6], [9]

$$\Phi_{N+} = \frac{2kT}{q} \ln \frac{2d_{drift}}{\pi L_D} \tag{8}$$

with $L_D = \sqrt{2\epsilon_{drift} kT/q^2 n^+}$ being the Debye length of the N^+-region. This formulation covers several types of barriers which are listed in Table II and will be further discussed below. In particular we refer to the triangular barrier created by the sheet doping in all-GaAs material, i.e., $\Phi_D = 0$, as a Mott barrier.

As the capacitance changes, the series resistance changes, too, as shown in Fig. 4. The maximum,

$$R_{max} = 2R'_{max} + R_{N+}, \tag{9}$$

is the resistance of both drift regions in accumulation plus the parasitic series resistance, whereas the minimum,

$$R_{min} = R'_{max} + R_{N+}, \tag{10}$$

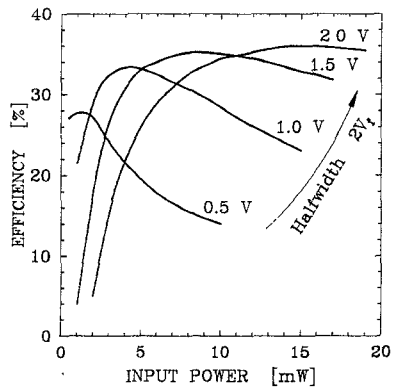

Fig. 6. Simulated efficiency for BIN tripler to 200 GHz as function of input power with halfwidth of $C - V$ as parameter. $C_{max} = 15$ fF, $C_{min} = 5$ fF, $R = 20\ \Omega$.

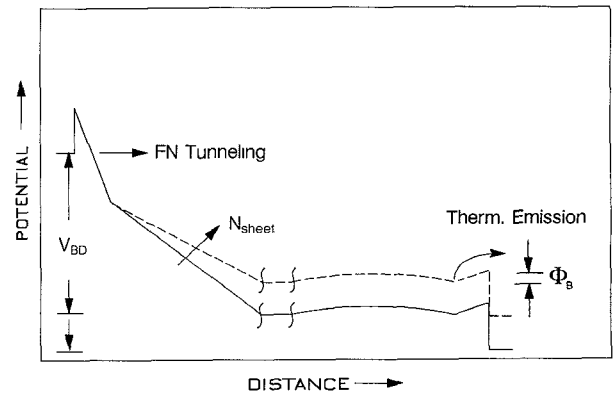

Fig. 7. Potential distribution in back-to-back BIN at breakdown, voltage V_{BD}. Increased sheet doping decreases V_{BD}.

is the resistance of only one accumulated diode plus parasitic because the other diode is fully depleted. As a reasonable average value we have used $R = 1.5R'_{max} + R_{N+}$ in the simulations.

Fig. 6 shows a simulated result for a tripler to 200 GHz. For a given halfwidth $2V_f$ the efficiency η peaks at a certain input power with the peak shifting to higher powers, broadening, and reaching a saturation value for larger halfwidths. Furthermore, the input power is related to the peak voltage drop over the capacitance, $\hat{V}_C$, by $P_{in} \propto \hat{V}_C^2$. The condition for maximum efficiency, obtained from many simulations, can be described by

$$2V_f = 0.6 \frac{C_{min}}{C_{max}} \hat{V}_C, \tag{11}$$

where $2V_f$ should be much larger than kT/q for a BIN structure.

The question of what limits $\hat{V}_C$ is investigated in Fig. 7. Here the conduction band edge of a back-to-back BIN structure with Mott barriers and a 100-nm drift region has been plotted from a PISCES [7] simulation depicting the situation 10 ps after the application of a large voltage step. (The steady-state solution differs by a decreased voltage drop over the forward biased barrier due to a substantial conductance.) The fields are high in the reverse biased and low in the forward biased diode as long as the input frequency is much smaller than the cut-off frequency.

The forward biased barrier exhibits a current of density, see, e.g., [8],

$$j_{TE} = \frac{4\pi q m_{bar} k^2 T^2}{h^3} \exp\left\{-\frac{q\Phi_B}{kT}\right\}, \tag{12}$$

which is caused by thermionic emission (TE) over the barrier with m_{bar} being its effective mass and Φ_B its effective height, which may be voltage dependent. The current in the reverse biased barrier is dominated by Fowler–Nordheim (FN) tunneling with a density [8]

$$j_{FN} = \frac{m_0}{m_{bar}} \frac{q^3 E_{bar}^2}{8\pi h \Phi_M} \exp\left\{-\frac{8\pi\sqrt{2m_{bar}q}\,\Phi_M^{3/2}}{3hE_{bar}}\right\}, \tag{13}$$

which, in contrast to the thermionic current, is a strong function of the field in the barrier, $E_{bar} > 0$. As a consequence, the "reverse" current rises very sharply with the total applied voltage and will overtake the "forward" current at a "breakdown" voltage. Beyond that voltage, the barriers would become highly rectifying in a sense that would lead to a build-up of charge between the barriers, which would shift the flatband voltage.[2]

We estimate this functional breakdown voltage by equating the exponents of (8) and (9). This leads to the barrier breakdown field

$$E_{bar,BD} = \frac{8\pi\sqrt{2m_{bar}q\Phi_M}}{3h} \frac{\Phi_M}{\Phi_B} \frac{kT}{q}, \tag{14}$$

which at $T = 300$ K reduces to

$$E_{bar,BD} = \frac{1.7 \times 10^6}{\mathrm{V}^{1/2}\,\mathrm{cm}} \sqrt{\frac{m_{bar}}{m_0}}\,\Phi_M \frac{\Phi_M}{\Phi_B}. \tag{15}$$

As inferred from the simulation of Fig. 7, the effective height of the Mott barrier is around 0.3 V.

The above derivation of the breakdown holds not only for (triangular) Mott barriers but also for the trapezoidal heterojunction and oxide barriers as long as these barriers are not so thin that the current tunnels through the full barrier at breakdown, i.e., $\Phi_M - E_{bar,BD}\, d_{bar} \leq 0$ must be fulfilled. For these trapezoidal barriers, which conduct only a little in forward direction, we estimate $\Phi_B \approx \Phi_D$, as the voltage drop over the forward biased diode will be about V_f, which will usually be larger than $\Phi_M - \Phi_D$, cf. Fig. 5.

The breakdown voltage of a single diode is related to the barrier breakdown field by

$$V_{BD,s} \approx E_{bar,BD}\left(\frac{\epsilon_{bar}}{\epsilon_{drift}} d_{drift} + d_{bar}\right) - \frac{qN_{sheet}}{\epsilon_{drift}} d_{drift} + \Phi_D - \Phi_M. \tag{16}$$

[2]This charge accumulation breakdown voltage is unique to the back-to-back barrier diode structures. It competes with the voltage at which the leakage current in the barrier becomes equal to the displacement current, i.e., $j_{FN} = \omega\epsilon_{bar}E_{bar}$, which happens at a somewhat larger voltage in the cases considered here.

By applying $Q = \int C\, dV$ to the single and the back-to-back diodes, the breakdown voltage of the latter is obtained as

$$V_{BD} \approx \frac{C_{\min,s}}{C_{\min}} (V_{BD,s} - V_f) + 2V_f \tag{17}$$

with

$$\frac{C_{\min,s}}{C_{\min}} = \frac{d_{\text{bar}}}{d_{\text{bar}} + d_{\text{drift}}} + 1. \tag{18}$$

This derivation assumes that the voltage drop over the barriers is still determined by their capacitance rather than their conductance, which is a good approximation for heterojunction barriers at high frequency operation. Note the decrease of V_{BD} with increased sheet doping as illustrated in Fig. 7.

Table II lists the properties of various barriers starting with the simple GaAs Mott barrier, suitable only for low power applications, and progressing to AlGaAs/GaAs with about 50% Al, AlAs/GaAs, and SiO_2/Si. The Schottky barrier heights Φ_M of the III-V compounds have been estimated by the 2/3-bandgap rule. Note that tunneling through the X-valley is facilitated by the isotropic momentum distribution in the metal, which limits the advantage of a pure AlAs barrier.

With these parameters and the maximum allowed voltage drop over the capacitance, max ($\hat{V}_C$), set equal to V_{BD}, the results for the AlGaAs/GaAs heterojunction BIN tripler in Table III have been obtained. The area has been chosen to achieve matchable impedance levels.

TABLE II
PROPERTIES OF VARIOUS BARRIERS

Barrier Type	B-Material	Drift Region	Φ_M[V]	Φ_D[V]	m_{bar}/m_0
Mott	GaAs	GaAs	0.8	0	0.07
Heterojunction	AlGaAs	GaAs	1.2	0.4	0.10
Heterojunction	AlAs	:Γ GaAs	2.0	1.0	0.15
	AlAs	:X GaAs	1.4	0.6	0.19
Oxide	SiO_2	Si	3.2 $\cdots$ 4.1	3.2	1.0

TABLE III
SIMULATED PERFORMANCE OF A AlGaAs/GaAs BIN TRIPLER TO 200 GHz

d_{bar} [nm]	20
d_{drift} [nm]	80
N_{sheet} [cm^{-2}]	5.5×10^{12}
A [μm^2]	6
$C_{\max}$ [fF]	15
$C_{\min}$ [fF]	5
R [Ω]	20
$2V_f$ [V]	2.0
$\hat{V}_C$ [V]	11.5
P_{in} [mW]	19
η [%]	35.5
P_{out} [mW]	6.7
R_1 [Ω]	48
X_1 [Ω]	300
R_3 [Ω]	35
X_3 [Ω]	50

III. BARRIER-N-N^+ (BNN) MULTIPLIERS

If enough bulk doping N is added to the drift region (BNN diode), the current is no longer space charge limited. The resistance of the undepleted drift region becomes

$$R'_{\max} = \rho d_{\text{drift}}/A, \tag{19}$$

where $\rho = 1/qN\mu$ is the resistivity, which in turn depends on the doping and the electron mobility. The intrinsic cut-off frequency becomes

$$\omega_{ci} = 1/R'_{\max} C'_{\min} = 1/\epsilon\rho, \tag{20}$$

i.e., determined by dielectric relaxation. Unfortunately the mobility and with it the relaxation time degrades when the field in the drift region exceeds a critical field, E_{crit}. Although the mobility has a complex functional dependence on the spatial and temporal distribution of the electric field, we use a simple monotonic model

$$\mu(E_{\text{drift}}) = \frac{\mu_0}{1 + E_{\text{drift}}/E_{\text{crit}}} \tag{21}$$

with a properly adjusted $E_{\text{crit}} = v_s/\mu_0$ as an engineering guide. The design goal is to avoid $E_{\text{drift}} > E_{\text{crit}}$ as much as possible. Table I gives numerical values for the intrinsic cut-off frequency of BNN diodes with $N = 10^{17}/\text{cm}^3$ at low fields and the critical field. These cut-off frequencies are clearly much higher than the ones for the BIN diodes but are restricted to fairly low fields.

The transition from space charge limited behavior occurs when [9]

$$L_{\text{Debye}} = \sqrt{2\epsilon_{\text{drift}} kT/q^2 N} \le d_{\text{drift}}. \tag{22}$$

As a side effect, the transition from high to low capacitance becomes more gradual, i.e., with a long depletion tail, which can be described by

$$C' = \frac{C_{\text{bar}}}{\sqrt{1 + \alpha(V - V_f)}}, \tag{23}$$

where $\alpha = 2C_{\text{bar}}^2/qN\epsilon_{\text{drift}}A^2$. This approximation holds for $V \le V_f - 4kT/q$, where the flatband voltage is still given by (7), but now with

$$\Phi_{N+} = \frac{kT}{q} \ln N_c/N, \tag{24}$$

where N_c is the effective conduction band density of states. The spreading of the $C - V$ curve should have little effect on tripling for high enough powers as long as the diodes "punch through," i.e., the maximum depletion width reaches d_{drift}. If punch through is reached exactly when the barrier breaks down, then

$$V_{BD,s} \approx E_{\text{bar}} \left(\frac{\epsilon_{\text{bar}}}{\epsilon_{\text{drift}}} \frac{d_{\text{drift}}}{2} + d_{\text{bar}} \right) - \frac{qN_{\text{sheet}}}{\epsilon_{\text{drift}}} \frac{d_{\text{drift}}}{2} + \Phi_D - \Phi_M, \tag{25}$$

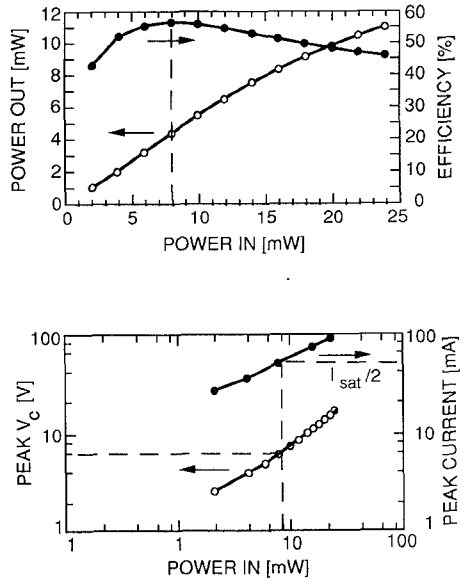

Fig. 8. Simulated performance of BNN tripler with C_{max} = 300 fF, C_{min} = 11 fF, R = 5 Ω. Simulation approximately valid up to a peak current of one half the saturation current, restricting input power to less than 8 mW (dotted lines).

TABLE IV
COMPARISON OF BIN AND BNN DIODES

BIN ($L_{Debye} \gg d_{drift}$)	BNN ($L_{Debye} \ll d_{drift}$)
Steep transition with largely constant slope $(dC/dV)/C = q/kT$	Gradual transition with long tail $C \propto 1/\sqrt{1 + \alpha(V - V_f)}$
High harmonic content even at low power	3rd harmonic little affected at high power
Space charge $n(x, V)$ injected into drift region from N^+	$n = N$ in undepleted drift region $n = 0$ in depleted part
$R'_{max} = d^2_{drift}/2\epsilon_{drift} v_s A$	$R'_{max} = d_{drift}(1 + E_{drift}/E_{crit})/qN\mu_0 A$
Transit time limited response $\omega_{ci} = 2v_s/d_{drift}$ for $E_{drift} > E_{crit} = v_s/\mu_0$	Relaxation time limited response $\omega_{ci} = 1/\epsilon\rho_0(1 + E_{drift}/E_{crit})$ with $1/\rho_0 = qN\mu_0$.
No space charge in depletion → average field at barrier	Positive space charge in depletion → higher than avg. field at barrier → lower breakdown voltage
Wide power range of moderate efficiency	Narrower power range of high efficiency

i.e., a reduction of almost a factor 2 in comparison to the BIN, if N_{sheet} is not reduced.

In our large signal simulations it was easier to monitor the total current rather than the field in the drift region. Since, according to (21), the current reaches 1/2 of its saturation value at the critical field, this should be the maximum current allowed to flow in the diode without serious degradation in the frequency response. Fig. 8 shows simulated results of a back-to-back AlGaAs/GaAs BNN tripler to 200 GHz with $N = 2.5 \times 10^{17}$ cm^{-3}, d_{bar} = 20 nm, d_{drift} = 100 nm, $N_{sheet} = 4 \times 10^{12}$ cm^{-2}, and A = 13 μm^2. The assumed series resistance of 5 Ω is largely due to the parasitic series resistance of the back region with $N^+ = 3 \times 10^{18}$/cm^3. Improved doping methods are likely to bring this resistance below 2 Ω. The maximum current is calculated as

$$I_{sat}/2 = qNv_sA/2 = 50 \text{ mA}. \quad (26)$$

This restricts the maximum input and output powers to P_{in} = 8 mW and P_{out} = 4.5 mW. A still higher doping of the drift region would cause the peak voltage to exceed the breakdown limit.

IV. Conclusions and Outlook

Table IV compares the properties of BIN and BNN diodes in summary form.

Despite the higher tripling efficiency of the BNN structure, its achievable output power per unit device area is not higher than that of the BIN. The power levels ($\propto A$) could be increased by increasing the area A if lower impedance levels ($\propto 1/A$) could be matched. Another approach would be to replace each BNN diode by a stack of several back-to-back BNN's in series in order to bring the impedance up again. Actually, no metal or N^+ layers would be necessary between barriers in each stack. The device approaches then the configuration of a stack of single barrier varactors [13] while preserving the planarity with Schottky contacts at the surface barriers. This Multi-Barrier-N-Barrier structure (BNB) is the subject of our ongoing analysis.

Whereas back-to-back BNN triplers are similar in their performance to overdriven Schottky barrier varactor triplers with carefully engineered back contacts and idlers [16], the Multiple BNB promises higher power capability while maintaining the simplicity of circuit integration.

We are presently implementing an AlAs/GaAs BNN tripler to 200 GHz with a target of 5 mW output power in a waveguide configuration with flip-mounting of a thinned chip to a quartz substrate, which carries the filter and coupling structures. We are also collaborating with Prof. N. C. Luhman and his students at UCLA on a quasi-optically coupled tripler array with an integrated antenna structure using the AlAs/GaAs system. Our analysis shows, however, that the SiO_2/Si BIN+ system should be revisited because of the theoretically superior breakdown resistance of the thin, grown oxide with no loss in saturation current at high fields in comparison to GaAs. Low yields due to oxide pinholes, that were experienced earlier [9], should be overcome due to improved cleanroom control.

Our simulation capability has been restricted to an input of a constant series resistance and a time-independent $C - V$ characteristic. We are presently interfacing the analysis program of Siegel and Kerr directly with an $I[V(t), t]$ device simulator, which calculates the current response $I(t)$ to any voltage waveform $V(t)$ as a function of time t. By this approach we avoid the introduction of a voltage dependent series resistance and a shunt capacitance, discrete equivalent devices which lose their physical meaning anyway when the Debye length is not small compared to the device length.

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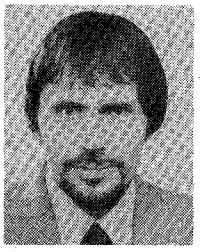

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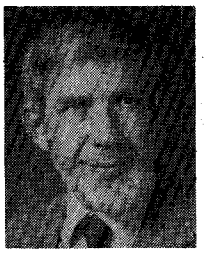

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